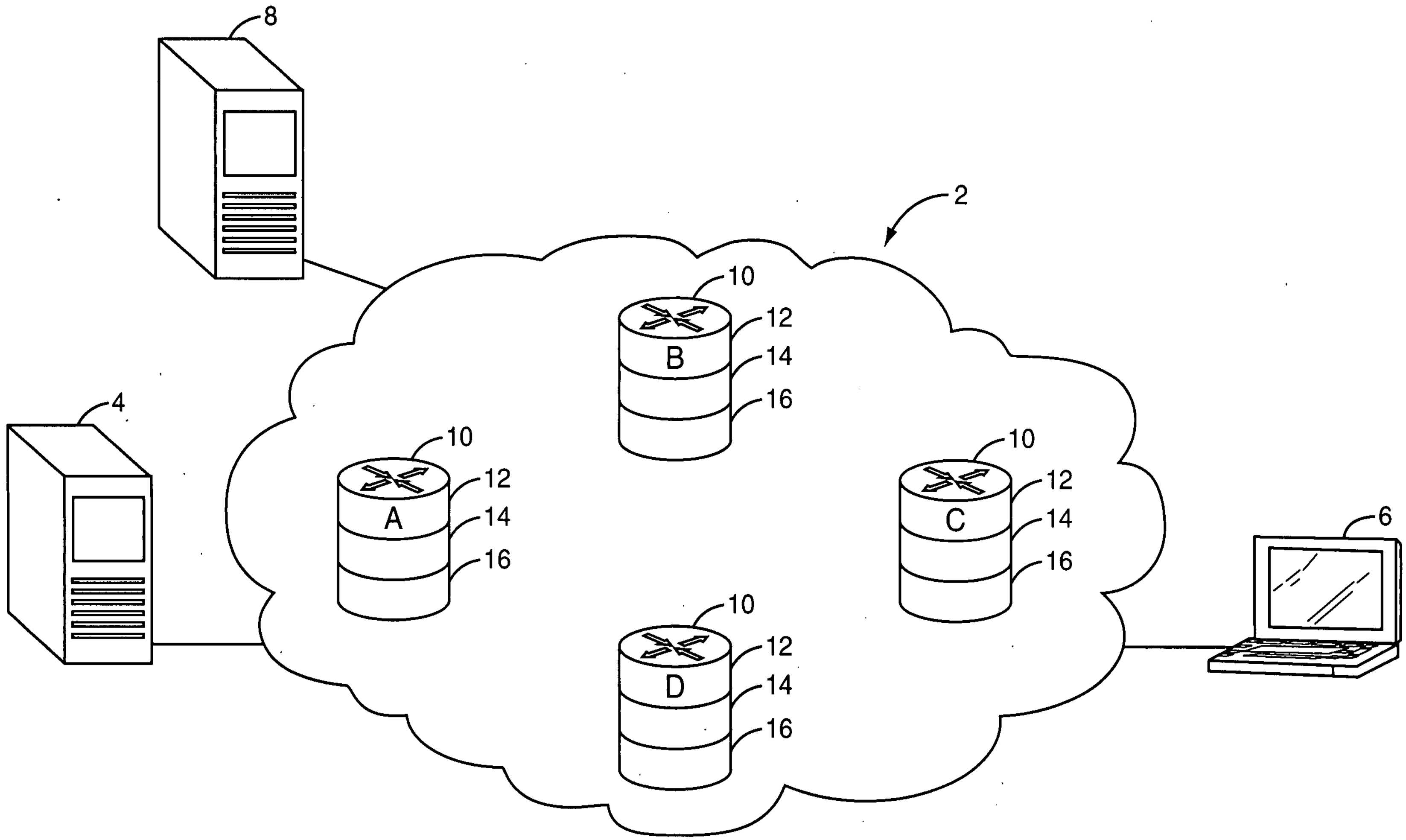

FIG. 1A

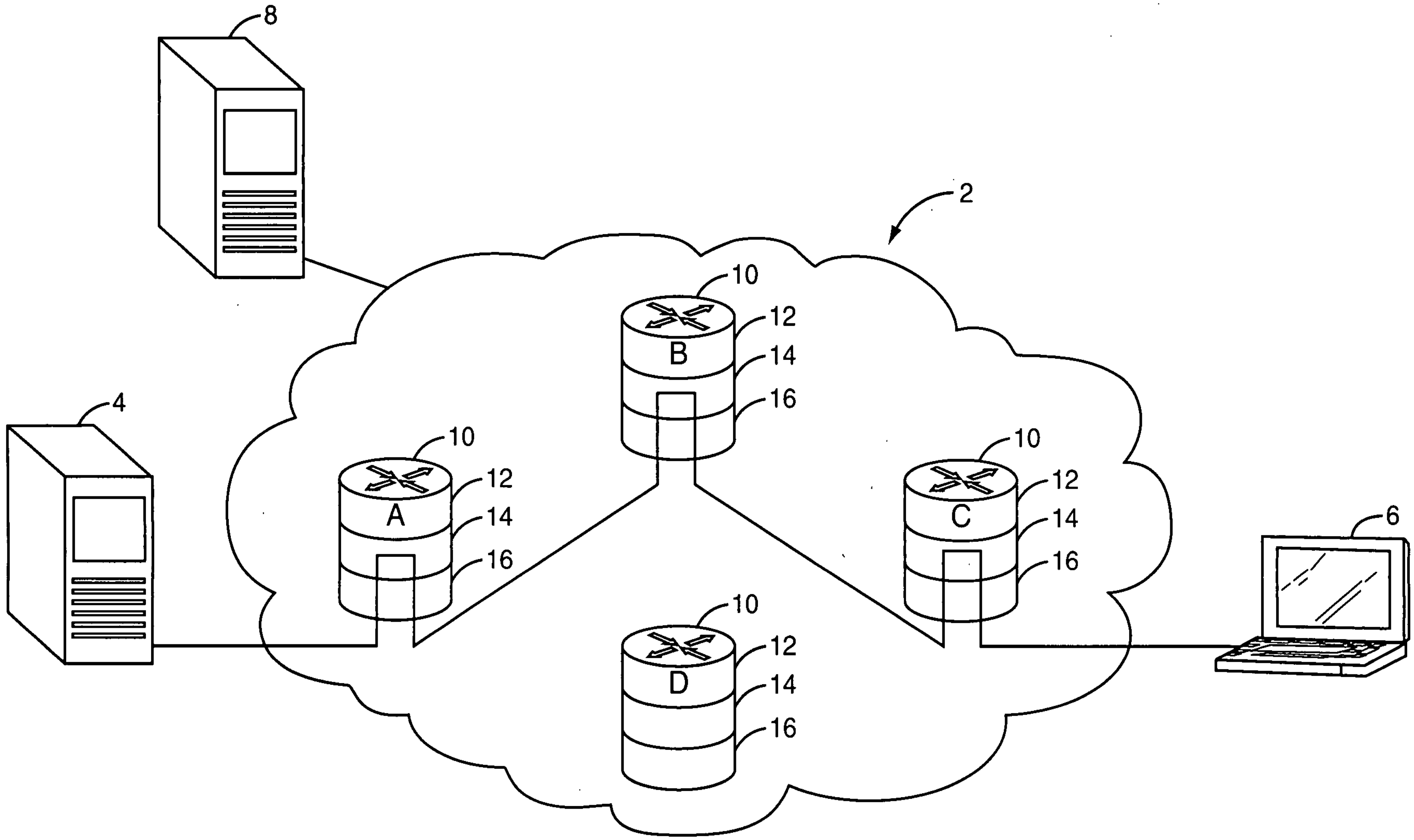

FIG. 1B

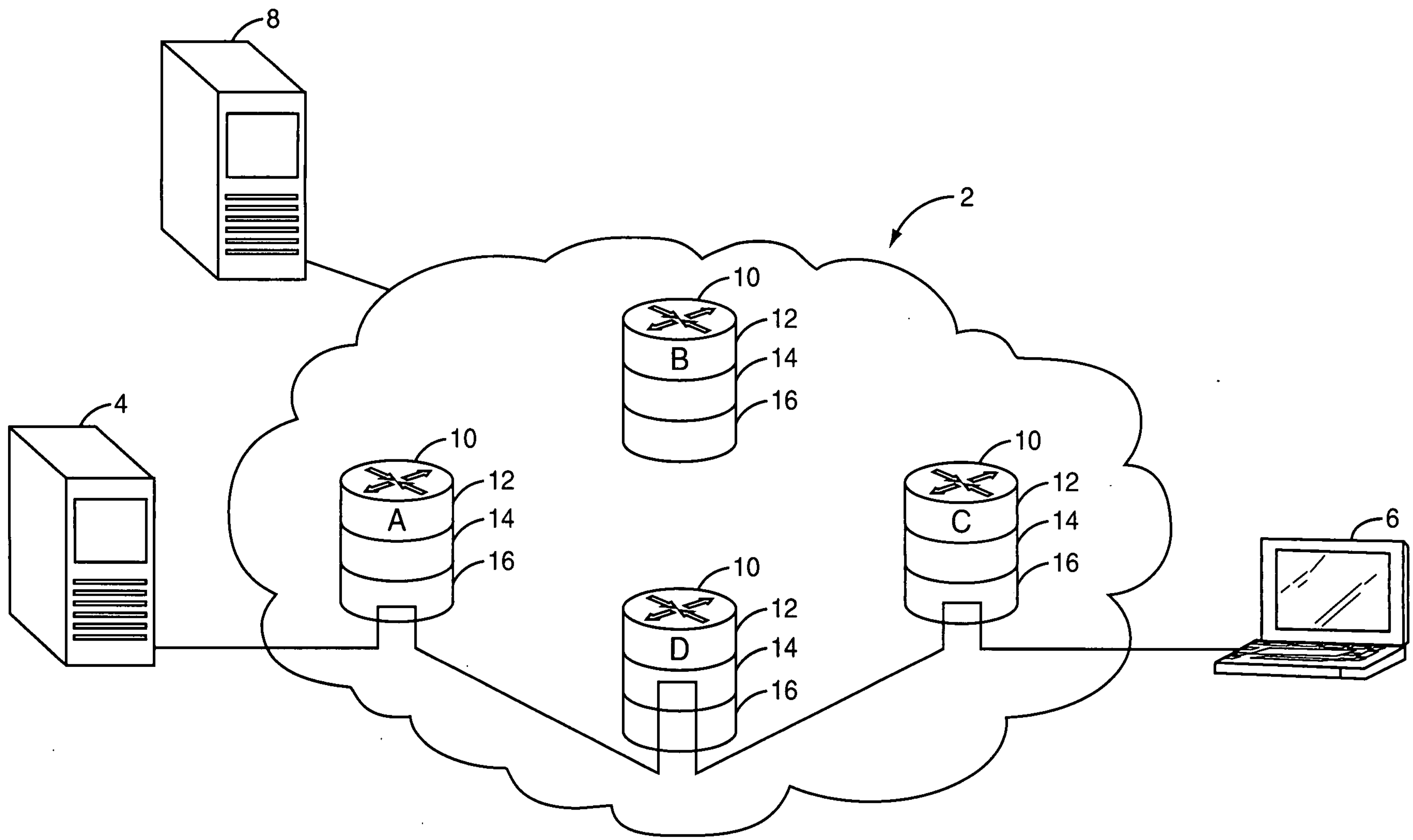

FIG. 1C

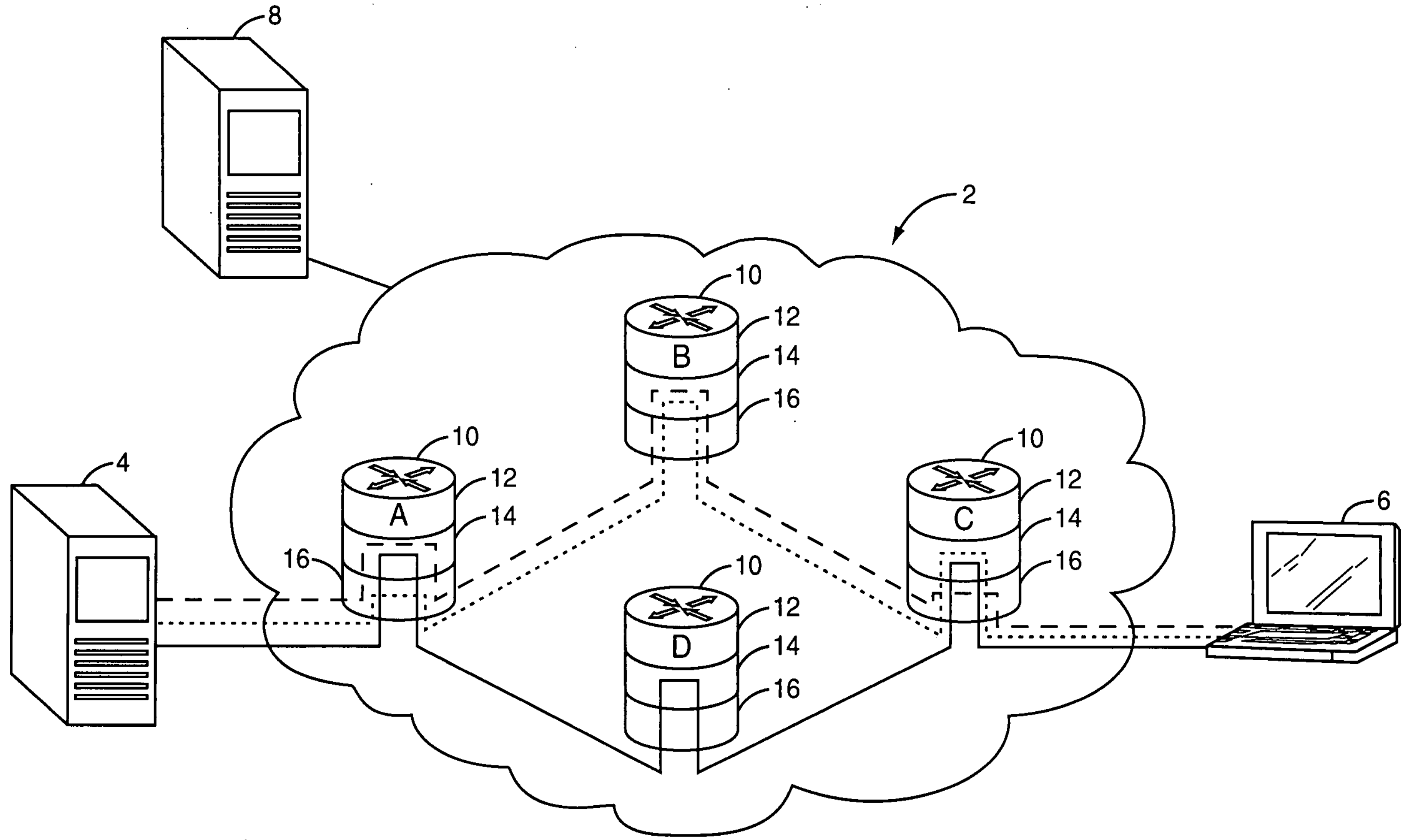

FIG. 1D

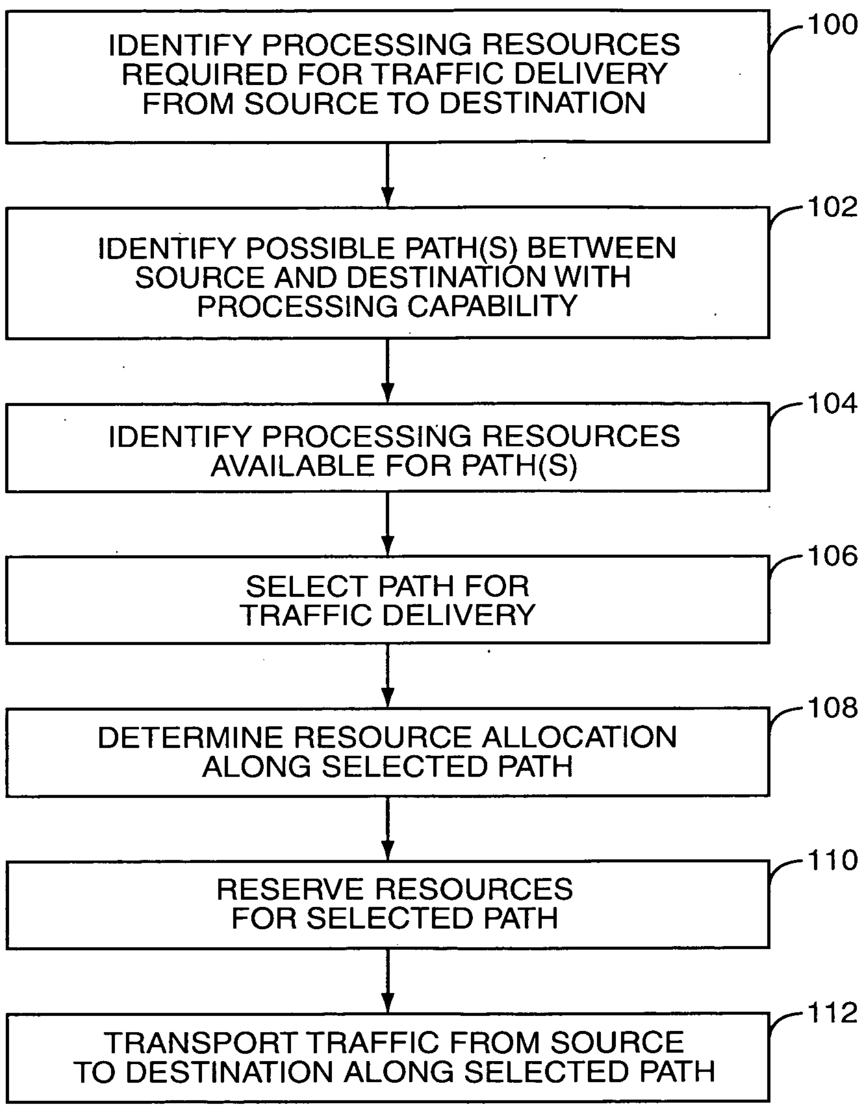
IDENTIFY PROCESSING RESOURCES REQUIRED FOR TRAFFIC DELIVERY FROM SOURCE TO DESTINATION
100
IDENTIFY POSSIBLE PATH(S) BETWEEN SOURCE AND DESTINATION WITH PROCESSING CAPABILITY
102
IDENTIFY PROCESSING RESOURCES AVAILABLE FOR PATH(S)
104
SELECT PATH FOR TRAFFIC DELIVERY
106
DETERMINE RESOURCE ALLOCATION ALONG SELECTED PATH
108
RESERVE RESOURCES FOR SELECTED PATH
110
TRANSPORT TRAFFIC FROM SOURCE TO DESTINATION ALONG SELECTED PATH
112

FIG. 2

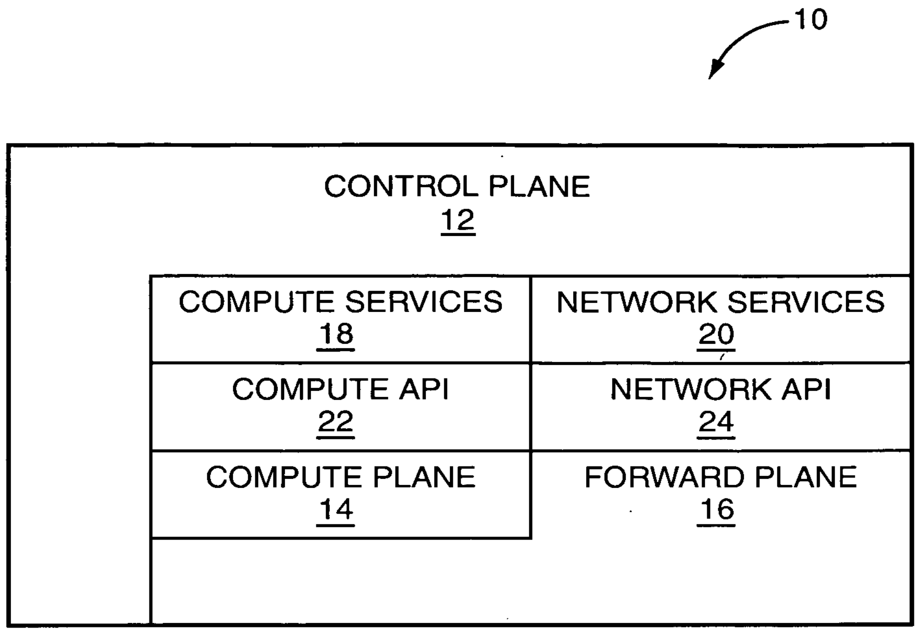
10
CONTROL PLANE
12
COMPUTE SERVICES
18
NETWORK SERVICES
20
COMPUTE API
22
NETWORK API
24
COMPUTE PLANE
14
FORWARD PLANE
16

FIG. 3

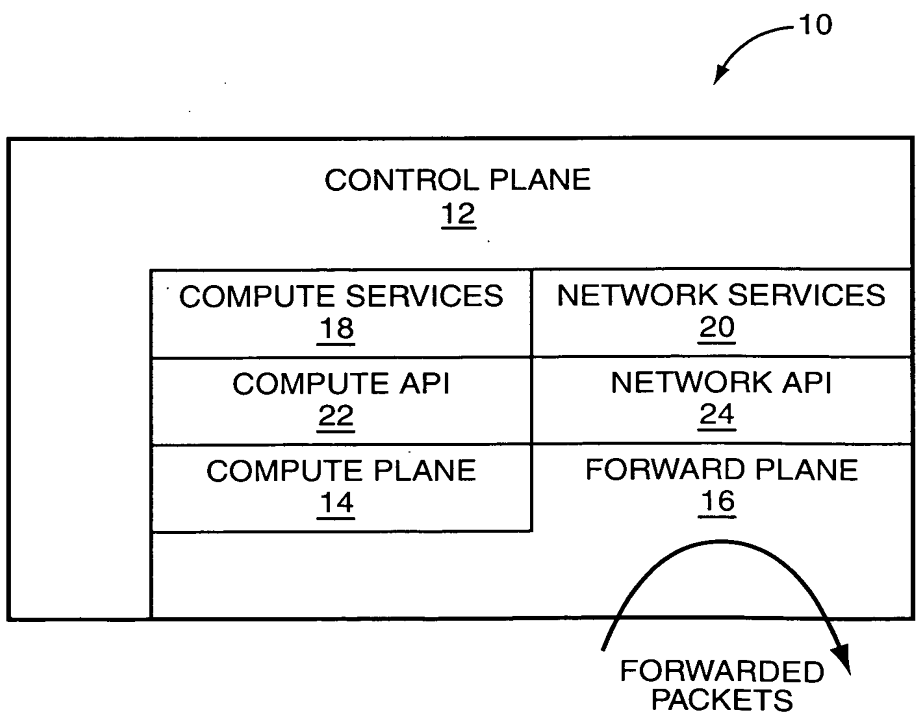
10
CONTROL PLANE
12
COMPUTE SERVICES
18
NETWORK SERVICES
20
COMPUTE API
22
NETWORK API
24
COMPUTE PLANE
14
FORWARD PLANE
16
FORWARDED
PACKETS

FIG. 4

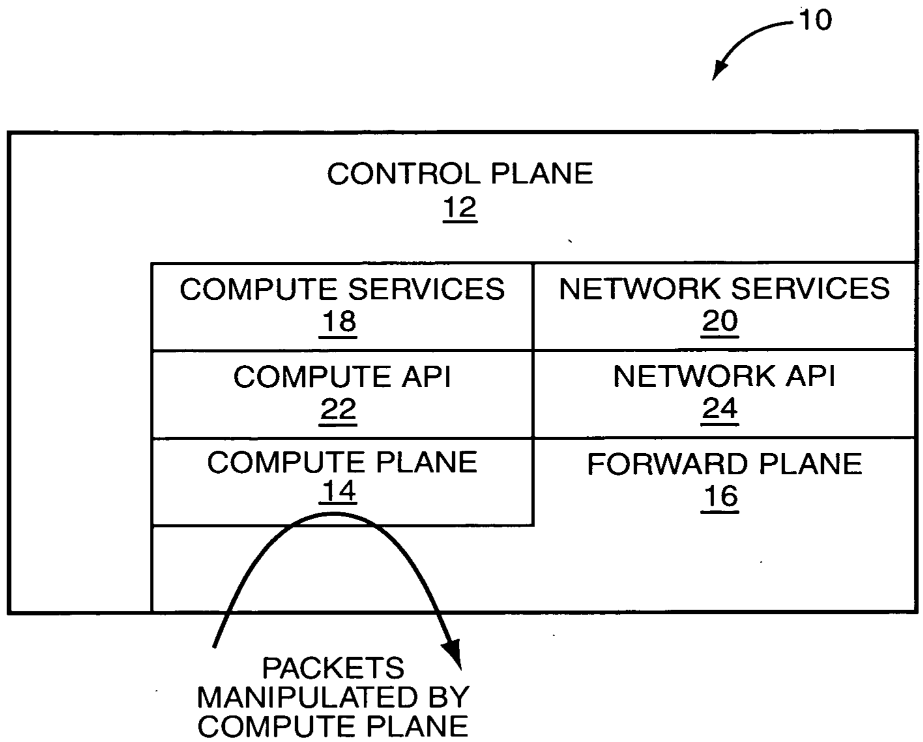
10
CONTROL PLANE
12
COMPUTE SERVICES
18
NETWORK SERVICES
20
COMPUTE API
22
NETWORK API
24
COMPUTE PLANE
14
FORWARD PLANE
16
PACKETS
MANIPULATED BY
COMPUTE PLANE

FIG. 5

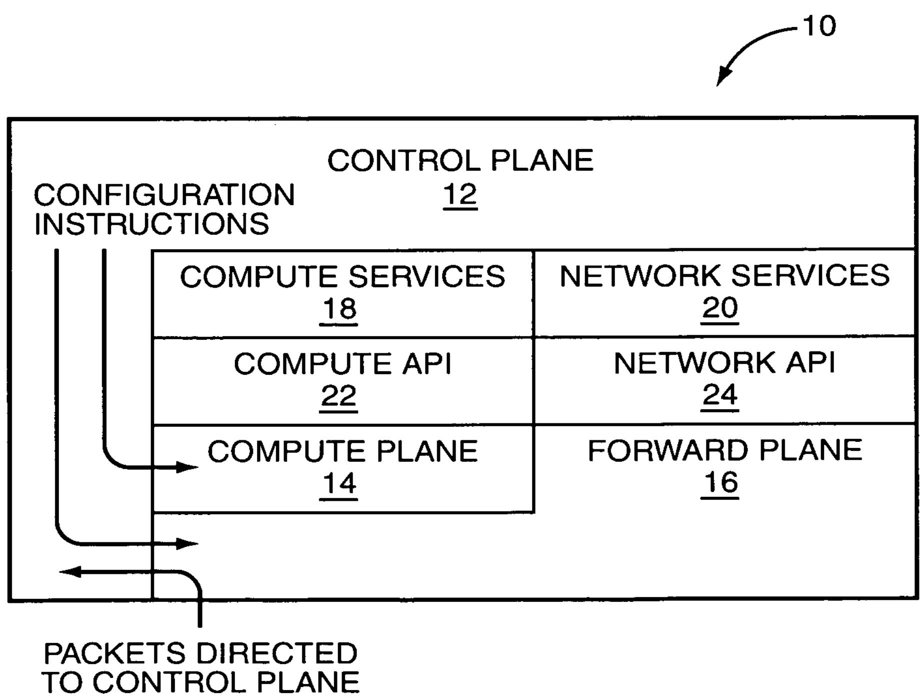
10
CONTROL PLANE
12
CONFIGURATION
INSTRUCTIONS
COMPUTE SERVICES
18
NETWORK SERVICES
20
COMPUTE API
22
NETWORK API
24
COMPUTE PLANE
14
FORWARD PLANE
16
PACKETS DIRECTED
TO CONTROL PLANE

FIG. 6

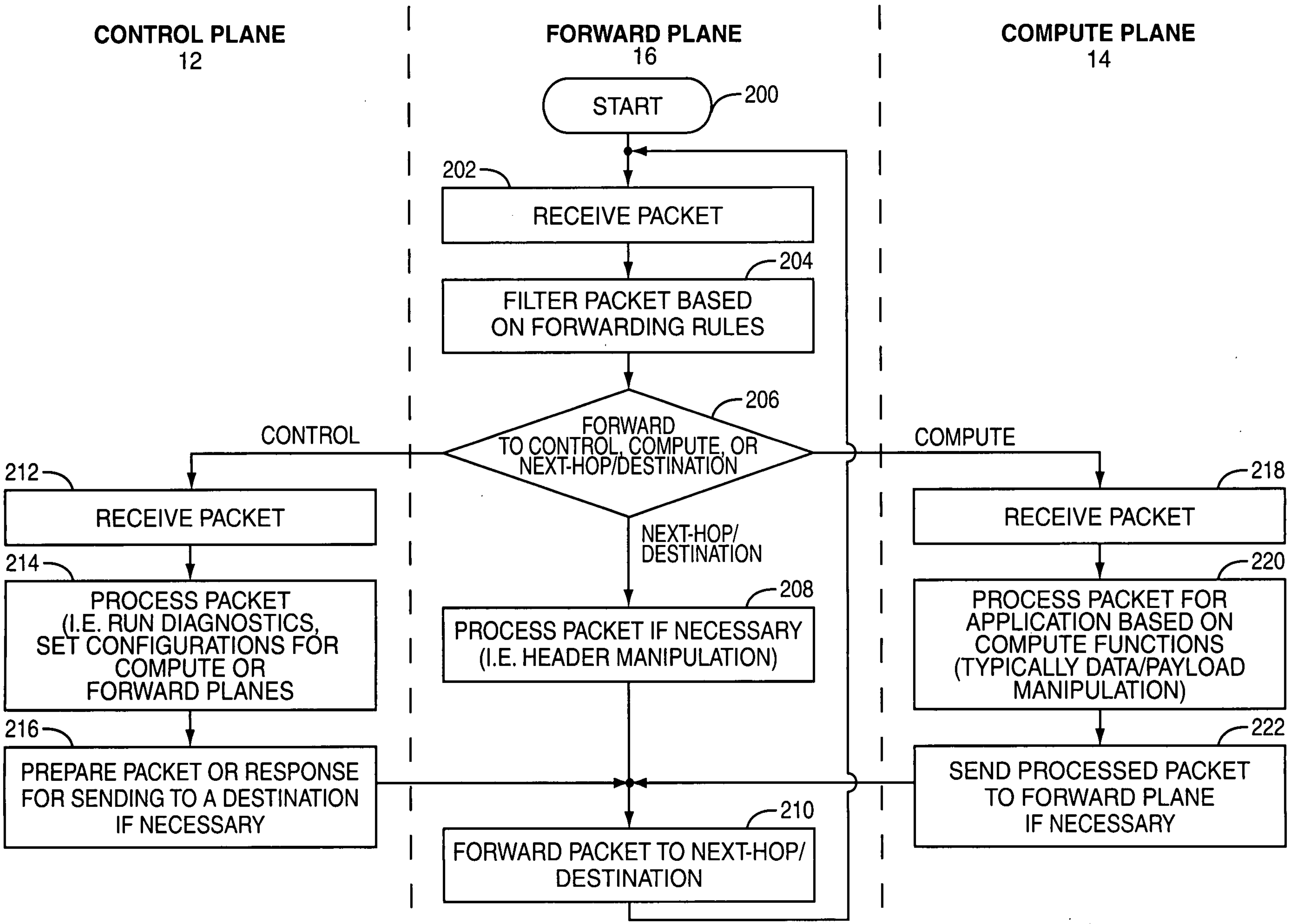
CONTROL PLANE
12
FORWARD PLANE
16
COMPUTE PLANE
14
START
200
202
RECEIVE PACKET
204
FILTER PACKET BASED ON FORWARDING RULES
206
FORWARD TO CONTROL, COMPUTE, OR NEXT-HOP/DESTINATION
CONTROL
COMPUTE
NEXT-HOP/ DESTINATION
212
RECEIVE PACKET
214
PROCESS PACKET (I.E. RUN DIAGNOSTICS, SET CONFIGURATIONS FOR COMPUTE OR FORWARD PLANES
216
PREPARE PACKET OR RESPONSE FOR SENDING TO A DESTINATION IF NECESSARY
208
PROCESS PACKET IF NECESSARY (I.E. HEADER MANIPULATION)
210
FORWARD PACKET TO NEXT-HOP/ DESTINATION
218
RECEIVE PACKET
220
PROCESS PACKET FOR APPLICATION BASED ON COMPUTE FUNCTIONS (TYPICALLY DATA/PAYLOAD MANIPULATION)
222
SEND PROCESSED PACKET TO FORWARD PLANE IF NECESSARY

FIG. 7

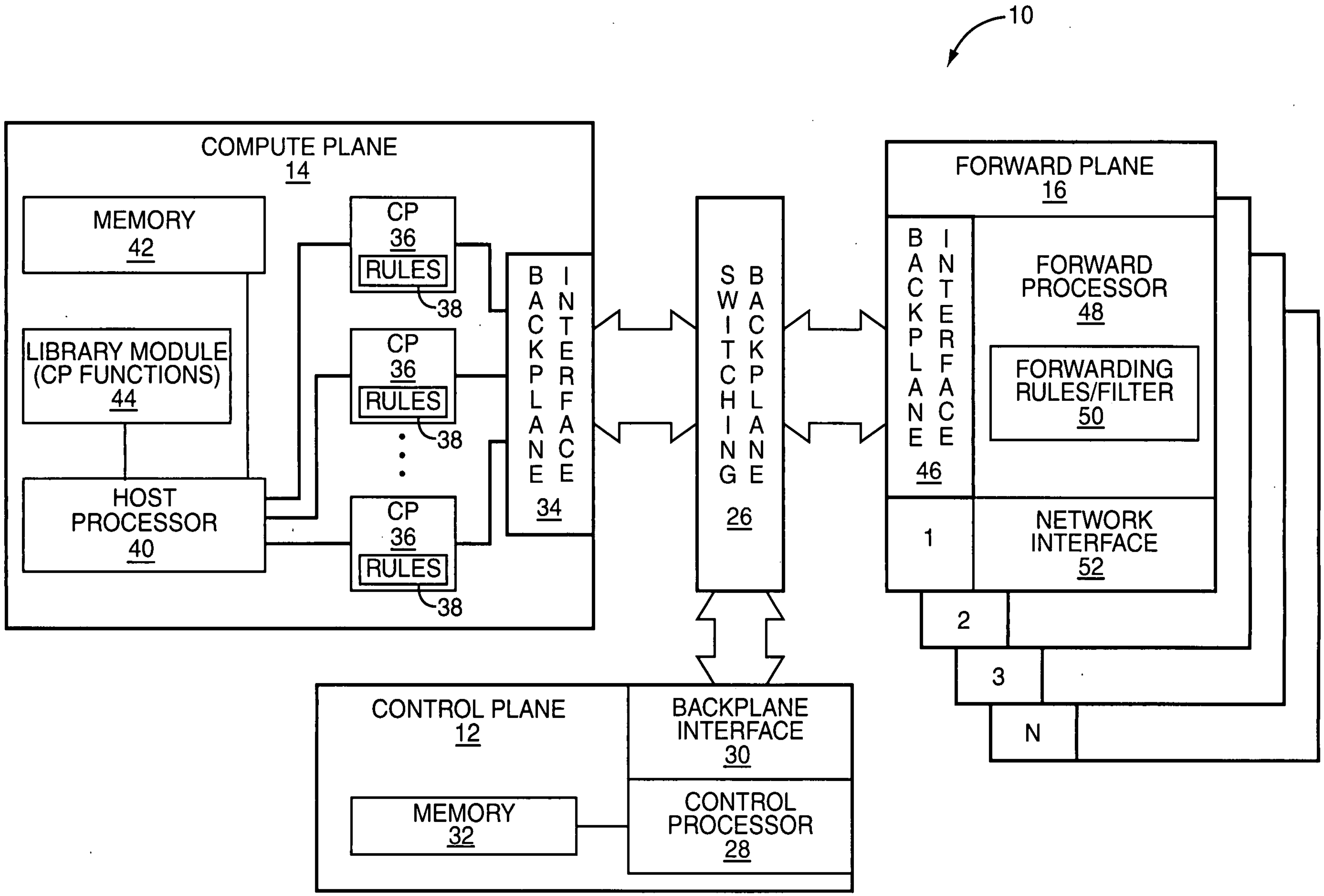
10
COMPUTE PLANE
14
MEMORY
42
LIBRARY MODULE
(CP FUNCTIONS)
44
HOST
PROCESSOR
40
CP
36
RULES
38
CP
36
RULES
38
CP
36
RULES
38
BACKPLANE INTERFACE
34
SWITCHING BACKPLANE
26
FORWARD PLANE
16
BACKPLANE INTERFACE
46
FORWARD
PROCESSOR
48
FORWARDING
RULES/FILTER
50
1
NETWORK
INTERFACE
52
2
3
N
CONTROL PLANE
12
MEMORY
32
BACKPLANE
INTERFACE
30
CONTROL
PROCESSOR
28

FIG. 8